We claim:

1. A cache memory, comprising:

a plurality of cache lines for storing a value from main memory, at least one of said cache lines having an associated cache line decay interval; and

a timer associated with at least one of said plurality of cache lines, at least one of said timers configured to control a signal that removes power to said associated cache line after said cache line decay interval.

2. The cache memory of claim 1, wherein a timer associated with a given cache line is reset each time said associated cache line is accessed.

3. The cache memory of claim 1, wherein said cache line decay interval is adjusted based on a performance evaluation of said cache memory.

4. The cache memory of claim 1, wherein said cache line decay interval is increased following a cache miss for said associated cache line.

5. The cache memory of claim 1, wherein said cache line decay interval is decreased following a successful cache decay.

6. The cache memory of claim 3, wherein said decay interval adjustment is implemented by adjusting a reference value in a comparator.

7. The cache memory of claim 3 wherein said decay interval adjustment is implemented by varying the number of active bits in a local counter.

8. The cache memory of claim 3 wherein said decay interval adjustment is implemented with a plurality of global counters of different magnitude and a selection of the global timing signal for a given cache line that arrives at a local counter of a given cache line.

9. The cache memory of claim 1, wherein said timer is a k bit timer and said timer receives a tick from a global N-bit counter where k is less than N.

10. The cache memory of claim 1, wherein said timer receives a tick from a selected one of a plurality of global counters.

11. The cache memory of claim 1, further comprising a dirty bit associated with at least one of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval.

12. The cache memory of claim 1, wherein said removing power from said associated cache line resets a valid field associated with said cache line.

13. The cache memory of claim 1, wherein said timer is an analog device that detects a predefined voltage on said device corresponding to said decay interval.

14. A method for reducing leakage power in a cache memory, said cache memory having a plurality of cache lines, said method comprising the steps of:

resetting a timer each time a corresponding cache line is accessed;

removing power from said associated cache line after said timer reaches a cache line decay interval; and

adjusting said cache line decay interval for at least one of said cache lines based on an evaluation of a performance of said cache memory.

15. The method of claim 14, wherein said cache line decay interval is increased following a cache miss for said associated cache line.

16. The method of claim 14, wherein said cache line decay interval is decreased following a successful cache decay.

17. The method of claim 14, wherein said step of adjusting said cache line decay interval is implemented by adjusting a reference value in a comparator.

18. The method of claim 14, wherein said step of adjusting said cache line decay interval is implemented by varying the number of active bits in a local counter.

19. The method of claim 14, wherein said step of adjusting said cache line decay interval is implemented with a plurality of global counters of different magnitude and a selection of the global timing signal for a given cache line that arrives at a local counter of a given cache line.

20. The method of claim 14, wherein said timer is a k bit timer and said timer receives a tick from a global N-bit counter where k is less than N.

21. The method of claim 14, wherein said timer receives a tick from a selected one of a plurality of global counters.

22. The method of claim 14, further comprising a dirty bit associated with at least one of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval.

23. The method of claim 14, wherein said removing power from said associated cache line resets a valid field associated with said cache line.

24. The method of claim 14, wherein said timer is an analog device that detects a predefined voltage on said device corresponding to said cache line decay interval.

25. An integrated circuit, comprising:

a cache memory having a plurality of cache lines for storing a value from main memory, at least one of said cache lines having an associated cache line decay interval; and

a timer associated with at least one of said plurality of cache lines, at least one of said timers configured to control a signal that removes power to said associated cache line after said cache line decay interval.

26. The integrated circuit of claim 25, wherein said cache line decay interval is adjusted based on a performance evaluation of said cache memory.

27. The integrated circuit of claim 25, wherein said cache line decay interval is increased following a cache miss for said associated cache line.

28. The integrated circuit of claim 25, wherein said cache line decay interval is decreased following a successful cache decay.